Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **OUTPUT 1**
2. **INPUT 1-**
3. **INPUT 1+**
4. **Vcc**
5. **INPUT 2+**
6. **INPUT 2-**
7. **OUTPUT 2**
8. **OUTPUT 3**
9. **INPUT 3-**
10. **INPUT 3+**
11. **Vcc –**
12. **INPUT 4+**
13. **INPUT 4-**
14. **OUTPUT 4**

**.054”**

**.067”**

**2 1 14 13**

**12**

**11**

**10**

**3**

4

**5**

**6 7 8 9**

**3**

**4**

**8**

**A**

**MASK**

**REF**

**3**

**4**

**8**

**A**

**Top Material: Al**

**Backside Material: Si Ni**

**Bond Pad Size: .004” X .004”**

**Backside Potential: Vcc-**

**Mask Ref: 348A**

**APPROVED BY: DK DIE SIZE .054” X .067” DATE: 11/2/21**

**MFG: TEXAS INSTRUMENTS THICKNESS .025” P/N: LM148**

**DG 10.1.2**

#### Rev B, 7/19/02